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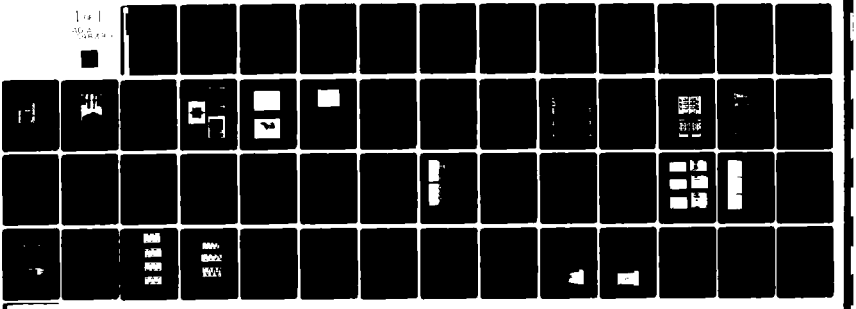

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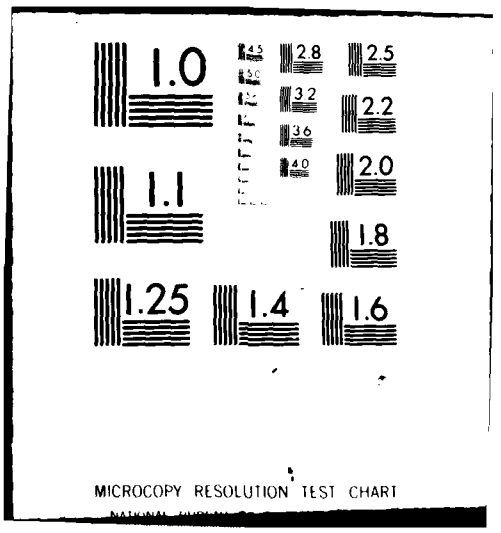
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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Efforts during the first year of this contract have concentrated on process development; material development and characterization; and circuit development. Preliminary results on single stage inverters show about a two-fold speed advantage at 77 K compared to that at 300 K for material doped in the mid - 10^{16} cm^{-3} range. This advantage is offset by a ~ 90% increase in power dissipation at 77 K compared to that at 300 K, so the speed-power product is approximately the same at the two temperatures. A more accurate assessment of circuit speed

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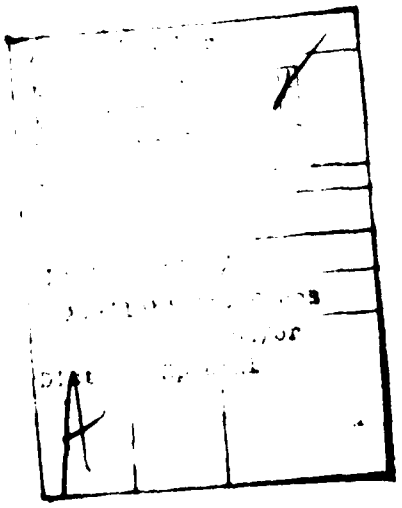
and power dissipation is expected by the use of ring oscillators. Accordingly, work has been concentrated in this area during the latter part of this period.



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LIST OF ILLUSTRATIONS
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ANNUAL TECHNICAL REPORT

FOR

GaAs FET LOGIC AT LOW TEMPERATURES

CONTRACT NO. N00014-79-C-0789

1 SEPTEMBER 1979 - 31 AUGUST 1980

SECTION I
INTRODUCTION

This report covers the progress made during the first year of a continuing research program, Contract No. N00014-79-C-0789, to investigate the potential speed advantages associated with the operation of GaAs integrated logic circuits at low temperatures (77 K). Research has been carried out in conjunction with an internally-funded program to develop a viable, room-temperature, high-speed GaAs logic technology. The material and processing technologies are being systematically developed for reproducibility, uniformity, and high yield appropriate for MSI circuit complexity. More recently, Texas Instruments has been awarded two Air Force programs (F33615-80-C-1171 and F33615-80-C-1047). The principal objective of the first program parallels that of TI's internally funded program. The principal objective of the second program is to develop the technology required for the design and fabrication of high density, high performance, low power GaAs integrated memory circuits. Progress made on these programs has contributed significantly to the present program and is expected to continue to do so. Therefore, in this report we will also cover related topics of importance to the present program.

SECTION II
MATERIAL DEVELOPMENT

A large number of GaAs epitaxial structures have been grown by vapor phase epitaxy on Cr-doped semi-insulating substrates during the past year. The doping concentration of the active layer encompassed the low 10^{15} cm^{-3} to the high 10^{16} cm^{-3} range. The active layers were grown on buffer layers having a typical thickness of approximately 3 μm. The surface morphology of the epitaxial layers has been very good. Van der Pauw mobility measurements on some of the slices have been made at 300 K and 77 K (see Figure 1). In general, the measured mobilities are comparable to those reported in the literature. Mobility ratios [$R_\mu = \mu(77\ K)/\mu(300\ K)$] between 3 and 4.5 are obtained for mid-10^{15} cm^{-3} doped active layers. This ratio decreases as the doping of the active layer increases. Mobility measurements using a fat-FET structure have been correlated to van der Pauw mobilities at both 300 K and 77 K. The two methods of measuring mobility agree to within ±15%.

The active layers were purposely grown thicker than required. Without anodic thinning, material uniformity is not adequate for circuit processing. Consequently, anodic thinning is employed to improve uniformity to an acceptable level (see Table 1). This procedure has also been applied to ~ 10^{16} cm^{-3} VPE layers with success. Using preliminary CV material characterization data, the slice is then uniformily etched to a thickness slightly greater than that appropriate for a pinch-off of -2.5 V. The desired pinch-off is subsequently achieved by a gate recess etch step.

Because it is plentiful, we have typically used anodically thinned VPE layers doped to ~ 10^{17} cm^{-3} for process and circuit development. More recently, the use of ion-implanted material in process development has increased because its reproducibility and uniformity have been favorable.

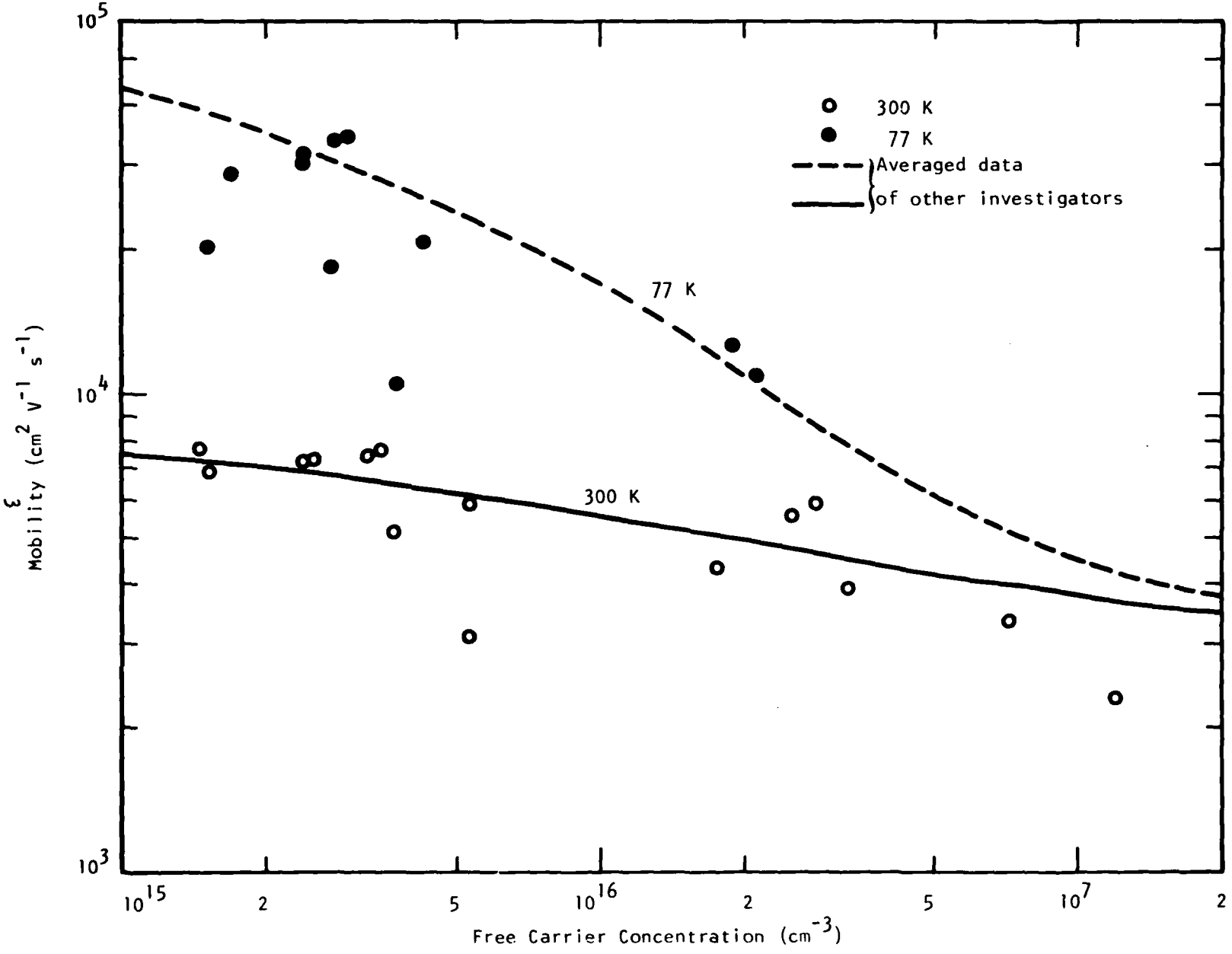


Figure 1 Van der Pauw Mobility Measurements of Vapor Phase Epitaxial Structures

Table 1

Long Range and Medium Range Uniformity Data

Lot No. 11

505 test FETs (W = 100 μm) : 4 x 5 master fields

	$I_{D\ max}$ (mA)	I_{DSS} (mA)	V_P (V)	g_m (ms)	ϕ (10^{12} cm^{-2})
Center	28	18.5	2.0	13.6	1.10
NE Corner	28	20	2.4	12.1	1.25
NW Corner	27	17	1.8	14.3	1.03
SW Corner	32	22	2.4	14.3	1.22
SE Corner	38	30	3.6	11.4	1.73

Test FETs (W = 100 μm) : Same master field near center of slice.

Field	$I_{D\ max}$ (mA)	I_{DSS} (mA)	V_P (V)	V_s (V)	R_{on} (Ω)	g_m (ms)
505	27.5	17.5	2.1	0.8	48	11
510	29.5	19	2.2	0.9	50	11
515	24.5	15	2.0	0.9	55	10
705	27.0	18.5	2.25	0.85	56	10
710	28.5	19	2.25	0.9	56	10.5
715	25.0	17	2.2	0.9	64	9

SECTION III
PROCESS DEVELOPMENT

The major part of our effort has concentrated on developing a standard, high-yield, reproducible fabrication process. The process, at present, is adequate for MSI (~ 80 gate) circuit complexity. This present standard process consists of device isolation, nitride patterning for e-beam alignment marks, ohmic contact formation, metallization for material characterization, gate delineation, first level metal, dielectric stand-off patterning, second level metal, and final encapsulation. Each step involves an average of about 20 separate operations. The steps are under adequate control for yields of ~ 70% for 12-stage inverter chains having 1.0 μm gates. Slice yields are ~ 50% with slice breakage being the dominant factor in yield loss. A brief discussion of the process steps follows.

A. Device Isolation

Anodically thinned VPE material was used during the initial stages of process development. The relatively thick active layer is conveniently isolated by mesa etching. This step is highly reproducible and is capable of accurately delineating 4 μm features. However, it has a minor drawback. The nonuniformity of the e-beam resist thickness at the mesa edge results in a tighter exposure window for 0.5 μm gate length circuits.

A second procedure for device isolation is B^+ isolation. This procedure is appropriate for the relatively thin (~ 0.3 μm) ion-implanted active layers. This procedure also is highly reproducible and is compatible with subsequent processing. When applicable, it is the preferred technique.

B. Nitride Pads For e-Beam Alignment Marks

This step involves delineation of large geometries. Occasionally, degradation of the e-beam alignment marks has been observed after alloying. We believe this is due to the nitride quality. A production-worthy plasma nitride deposition machine is presently being installed and is expected to improve nitride reproducibility.

C. Ohmic Contacts

The requirements for ohmic contacts are replication of small, closely spaced features; low contact resistance; contact uniformity (to the edges); reproducibility; high quality alignment marks; edge acuity; and adequate surface morphology. Although initially we experienced considerable difficulty with this process step, the current standard process adequately satisfies all these requirements. Figure 2 shows an ohmic contact test pattern and the subsequent gate level alignment to it. Such results are typical of the process which employs a Ni/AuGe/Ni metallization and a subsequent ~ 430°C alloying temperature cycle. No contact failure has occurred since the process has been standarized. It is worth mentioning that low contact resistance to mid -10^{15} cm^{-3} doped layer has also been obtained reproducibly.

After completion of this step, data are taken to characterize the contacts, the isolation, and the metallization resistance. In addition, data are taken to characterize the long-range, medium-range, and short-range material uniformity. Material with serious deficiencies is screened at this point.

D. Metallization for Material Characterization

Metallization for material characterization involves delineation of large geometries (> 5 μm). CV and fat-FET structures are fabricated. This step helps determine more precisely the amount of gate recess etching required to obtain the desired pinch-off voltage (and thereby improves slice yield).

Data taken at the completion of this step include a pinch-off voltage map and a CV profile map.

E. Gate Delineation

The Ti/Pt/Au gates are defined with e-beam lithography and lift-off. A dramatic improvement in yield over optical lithography was obtained for gate lengths of 2 μm or less. As noted earlier, care is required to delineate 0.5 μm gate lengths due to e-beam resist thickness variation at the mesa edge. Nevertheless, dual-gate FETs with 0.5 μm gates (100 μm wide) on a 1.5 μm center-to-center spacing can be formed with a visual yield of ~ 85% and an electrical yield of ~ 60% (see Figure 3).

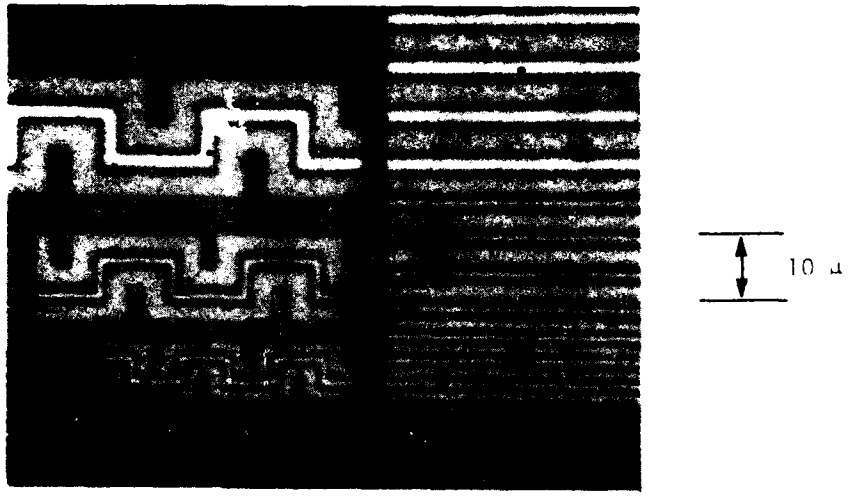


Figure 2 Ohmic/Gate Test Pattern. The duller appearing metal is the ohmic level; the brighter is the gate level. The pattern illustrates the replication of small, closely spaced ohmic features and the subsequent e-beam alignment to them.

Figure 3 SEM Photograph of Dual Gate Test [illegible] Slice 79B2-136). The gate lengths are 0.5 μm, and the source-drain spacing is 4 μm. Ohmic contacts are 0.1[illegible] thick; the gate metal is ~ 0.5 μm. Beam angle 60°. Length of bright line in lower right-hand corner is 1 μm.

The e-beam machine used, EBM-VI, is a fully automated production worthy instrument. Circuit geometries, obtained by automated techniques, serve as source input to a computer program which generates a pattern generator input tape for EBM-VI. The input tape is used to generate all GaAs logic optical mask levels and used for direct slice writing. Circuit modifications are rapidly implemented by altering the source file.

F. First Level Metal

A nitride assisted lift-off is employed for first level metal. The nitride also serves to passivate the GaAs surface of the active channels. Bar patterns of 2 μm lines and spaces are reproducibly delineated. Figure 4 shows representative structures that can be replicated with high yield even for a metallization thickness of ~ 5000 Å. The "rabbit-ear" problem, often observed with lift-off processes, has been significantly reduced by the processing procedure employed.

G. Dielectric Stand-Off

A ~ 1 μm thick polyimide layer is employed in this step. Test patterns consisting of 50 serially connected vias ranging from 1 to 5 μm by 8 μm are delineated. The underlying nitride layer is used to help determine when the vias are cleared. The yield of 50 serially connected 3 x 8 μm vias is typically ~ 50% while the yield of 4 and 5 μm vias is 90% and 100% respectively. Figure 5 shows SEM photographs of a portion of the via test pattern; the magnified view of one of the vias details the sidewall profile. The yield of 0.1 mm^2 overlay capacitors (another test pattern) is > 95%, suggesting a pinhole density < 50 cm^{-2}.

H. Second Level Metal

The Ti/Au metallization is patterned by lift-off. Bar patterns of 2 μm lines and spaces are reproducibly delineated (see Figure 6). Since the yield of stitch bonds to second level pads located atop the polyimide was not very high, these were relocated atop the nitride.

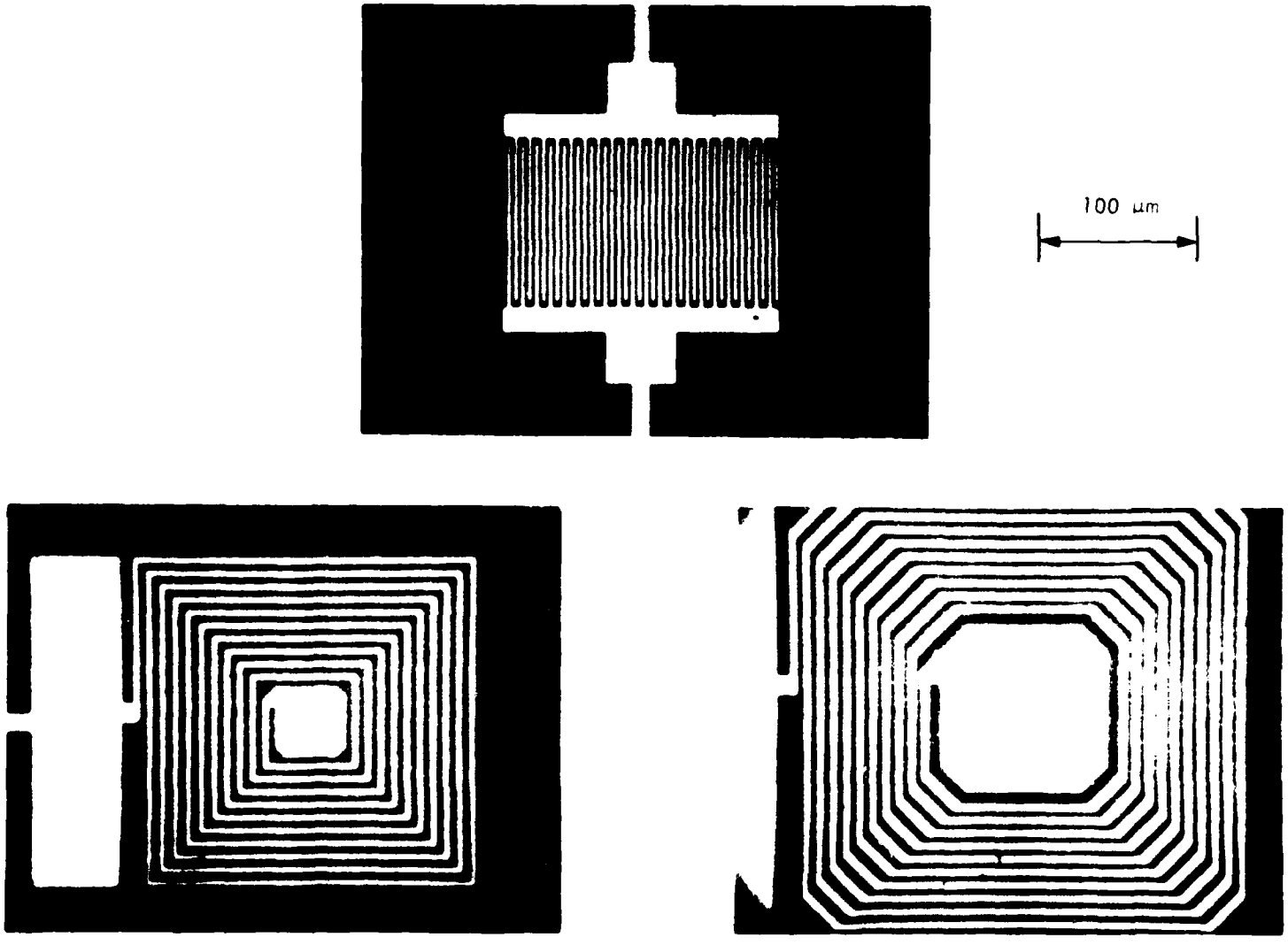


Figure 4 First Level Metal Test Structures

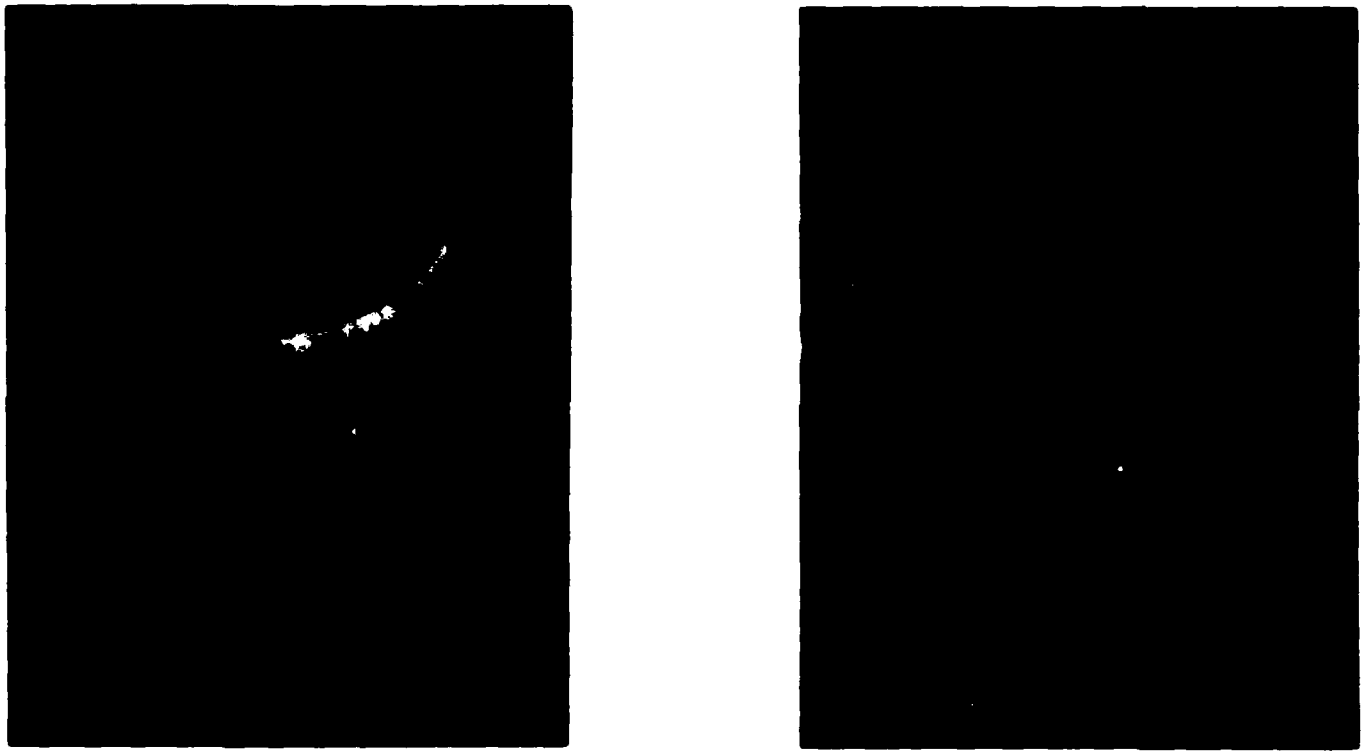


Figure 5 SEM Photographs of 4 x 8 μm Vias After Second Level Metallization

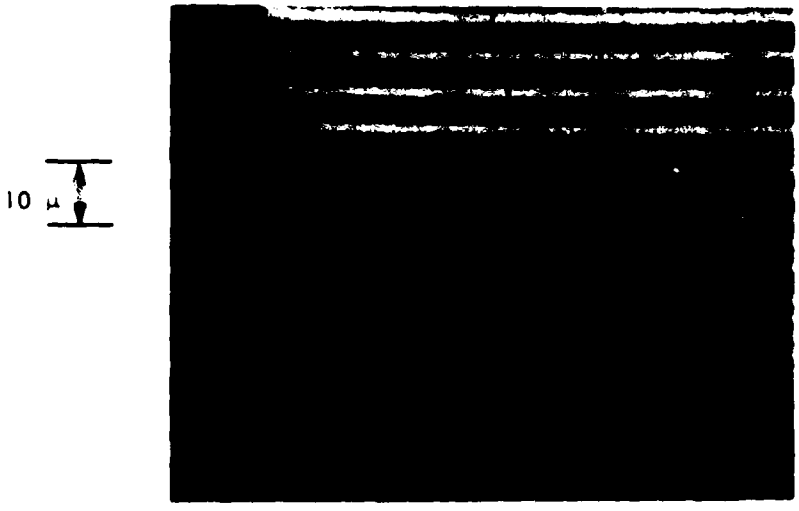


Figure 6 Second Level Metallization Bar Pattern Atop Polyimide

I. Final Encapsulation

Bonding pad openings in a second 1 μm thick polyimide are made for final encapsulation.

Although a considerable amount of progress in process development has been made during the past year, refinements in the standard circuit fabrication process are expected to continue during the next year.

We have performed some preliminary n^{++} ohmic contact studies. Room-temperature, low-energy, co-implants of Si + S, Si + Se, and Si + P, as well as Si alone were investigated. Several different implant doses were used for each case. Although definitive conclusions are not yet possible, the best results have been obtained with Si only implants. AuGe/Ni contacts were used, followed by sintering at 350°C. Results from these experiments have not been incorporated into the standard process because reproducibility has not yet been demonstrated.

SECTION IV
CIRCUIT DEVELOPMENT

Two mask sets, B and C, with the three inverter configurations shown in Figure 7 have been employed. The gate width of the switch FET (W_S) is 20 μm. Circuit (b) is a scaled-down version of the inverter configuration we had used earlier. Circuits (a) and (c) are configurations which have been analyzed in detail by Barna and Liechti.[1]

The first mask set (Mask B) uses the three circuits of Figure 7. Each 1.5 x 1.5 mm subfield contains one of each of the circuits. The master field consists of a 2 x 3 array of the subfields such that source-drain spacing of 5 and 7 μm and gate lengths of 0.5, 1.0 and 1.5 μm are obtained simultaneously. The gate level pattern is arranged to be compatible with minimum e-beam exposure time. Included in the master field are various test structures for material characterization and process development.

For further process development aimed at a high yield MSI capability, a second mask set (Mask set C) incorporating ring oscillators and advanced test structure was implemented. Figure 8 shows a mosaic photograph of the 6 x 6 mm master field of Mask set C, which is composed of a 3 x 3 array of subfields. The circuits contained in this master field are summarized in Table 2, and the location of the test patterns is indicated. The three inverter configurations of Figure 7 are arranged in 5-and 11-stage ring oscillators (ROs). Photographs showing the details of circuit layout are presented in Figure 9. The alphabetic character in the lower left-hand corner of each subfield corresponds to the inverter configuration defined by that figure. Going from bottom to top in each subfield, the gate lengths are 1.5, 1.0, 0.5, and 2.0 μm. From left to right, the fan-out loading is 1, 2, 4, and 8 [consisting of

[1]A. Barna and C. A. Liechti, "Optimization of GaAs MESFET Logic Gates with Subnanosecond Propagation Delays," J. Solid-State Circuits, SC-14, 708 (1979).

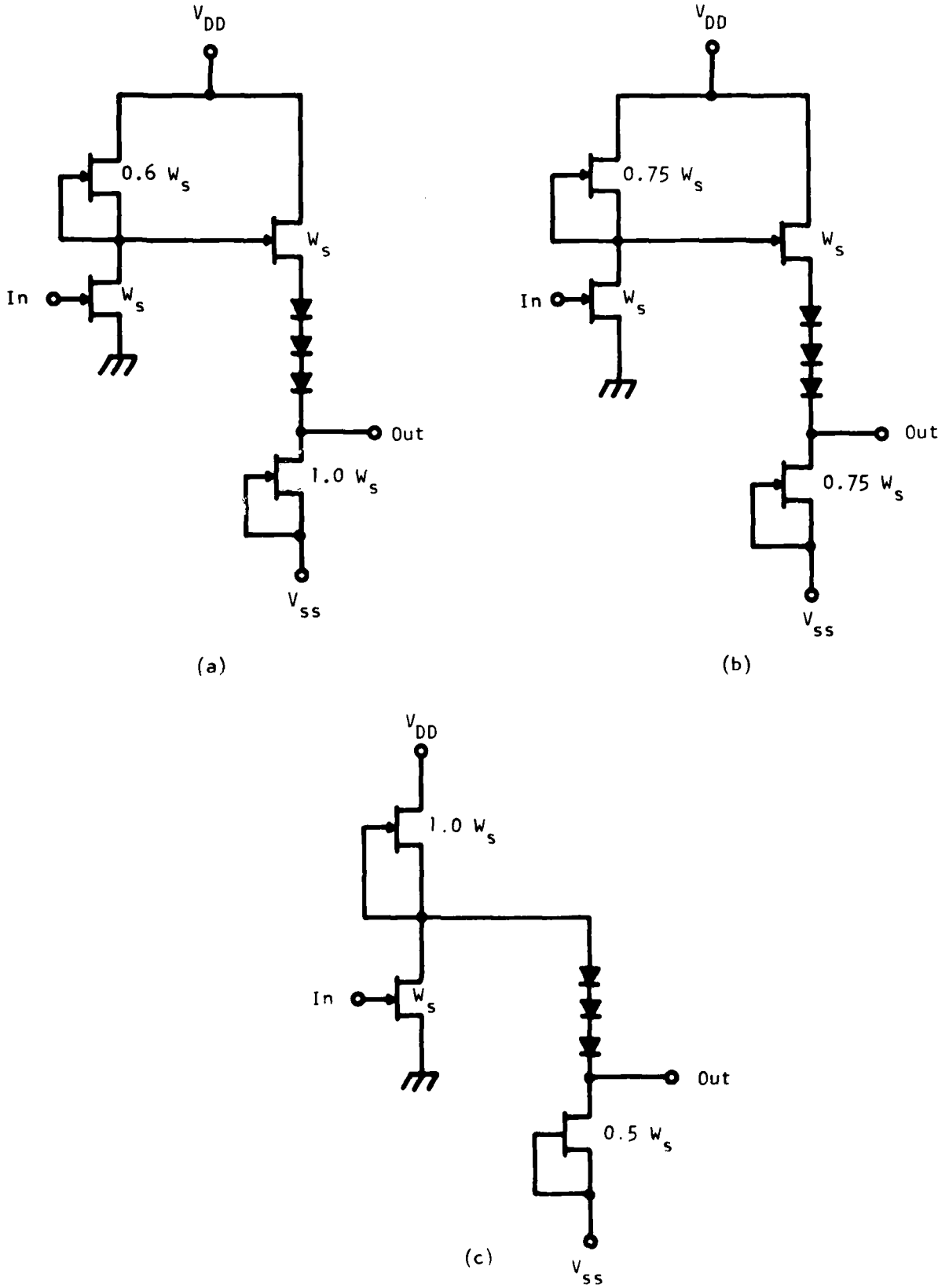


Figure 7 Inverter Configurations Employed in "Cold Logic B" Mask Set

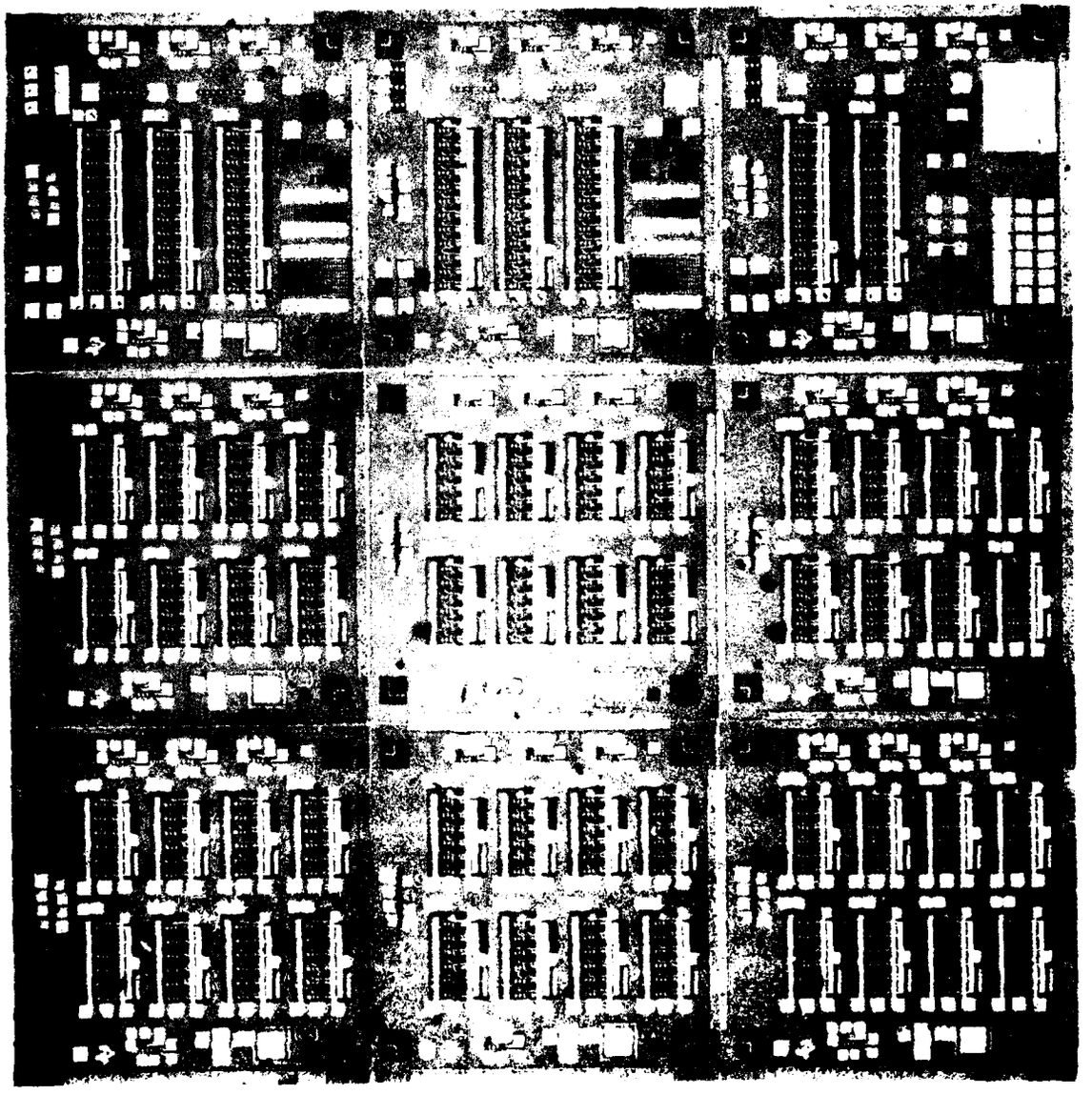


Figure 8 Logic C Master Field (6 x 6 mm)

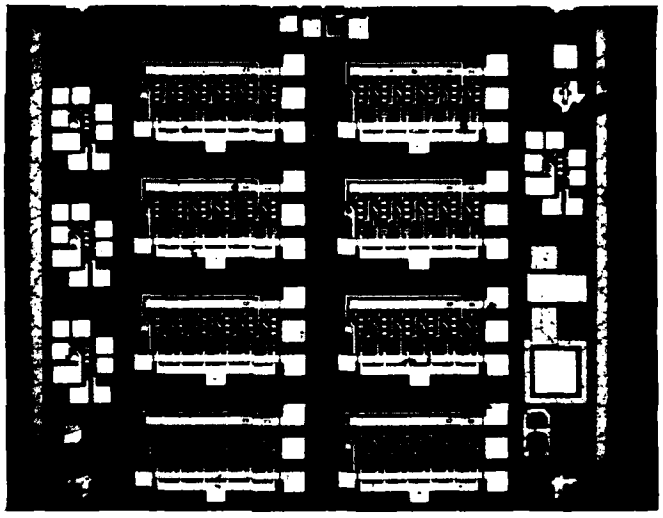
Table 2

Circuits and Test Patterns Contained on Mask Set C

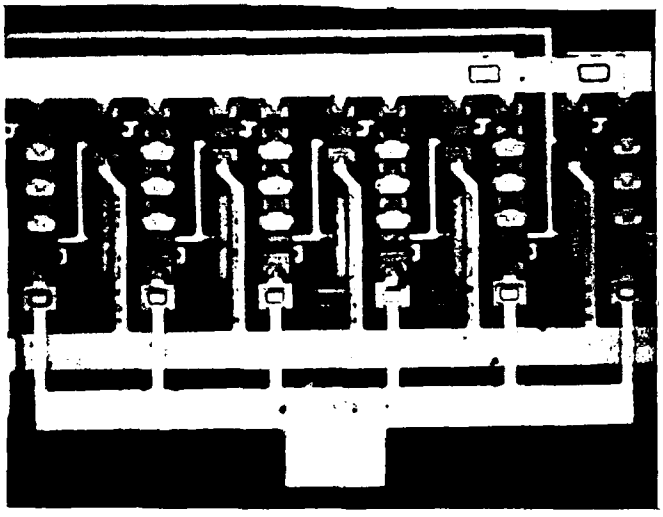
Mask Set C

- o 5-stage and 11-stage ring oscillators
- o 3 circuit configurations
- o 0.5, 1.0, 1.5 and 2.0 μm gate length circuits
- o Fan out of 1, 2, 4, and 8
- o Test Patterns
  - 10, 20, 40, 80, and 100 μm test FETs: top center - all subfields
  - Diode strings: NE - column 3
  - Single inverters: Periphery of all subfields
  - Van der Pauw: SE - C3
  - CV and fat-FET structure: WSW - all subfields
  - Contact resistance pattern: SW - A3
  - Isolation pattern (ohmic & Schottky): SW - A3
  - Meander lines (each level): lower center - A3
  - 2, 4, 6, 8, and 10 μm metallization interconnect pattern: S - B3 & C3
  - Metallization mimic: E - column 3
  - Gate alignment to ohmic contact pattern: S - B3 & C3
  - Bar patterns (each metallization level): S - B3 & C3
  - Crossovers (5 varieties): NW - column 3
  - Via test pattern: SW - B3 & C3
  - Via clear pattern: S - B3
  - Overlay capacitors: SE - A3
  - Interdigitated capacitor: SE - B3
  - Bar pattern for e-beam (each level): S - A3

Note: Column number is identified by the number of dots under the alphabetic character.

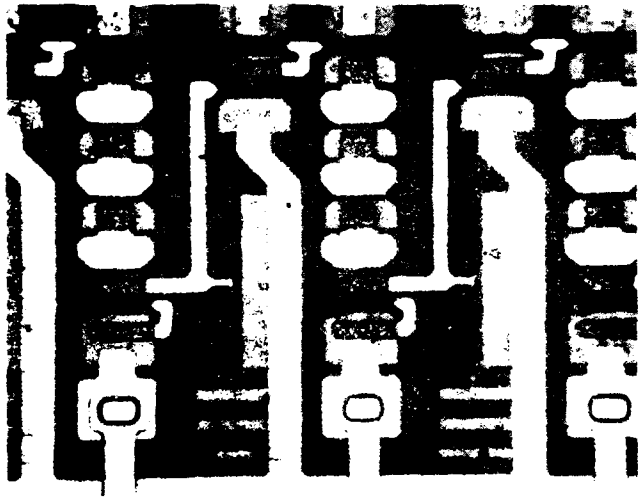


(a)

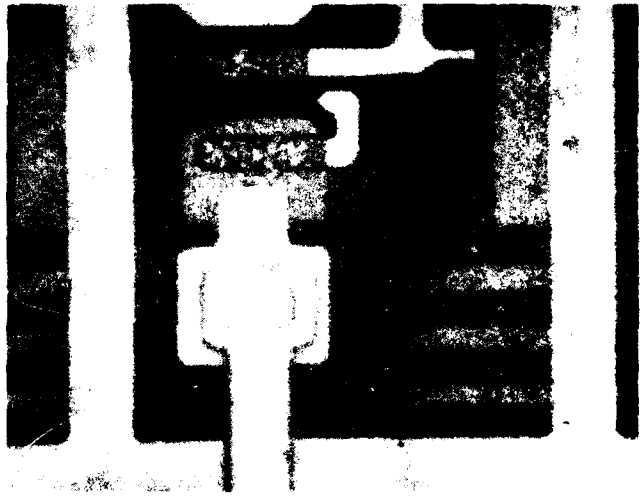


(b)

Figure 9 Detailed Views of Mask Set C Circuits



(c)



(d)

Figure 9 Continued

source-gate capacitances; see Figure 9(d)]. The 11-stage ROs in column 3 are used to confirm the propagation delays obtained from the five-stage ROs and for acquisition of yield and power dissipation data. Pads are provided to permit fabrication of ROs and/or inverter chains; these can be altered at will when the gate level pattern is delineated.

Mask set C includes four mask levels for experimental purposes. One level is for n^{++} ohmic contact studies. Another is for a deep implant to reduce the series resistance of the Schottky diodes. The remaining two mask levels are for investigating different alignment schemes so that subsequent levels can be aligned to the n^{++} implant.

SECTION V
ELECTRICAL CHARACTERIZATION

A. Slice Characterization

Electrical data is taken after certain steps in the fabrication sequence are completed. Table 3 summarizes data for a particular slice which was sheet implanted with Se at a dose of 5.0×10^{12} and 1.5×10^{12} cm^{-2} at 360 and 150 keV respectively. For device isolation, the B^+ -implant procedure was used. The slice was processed with a 500 Å gate recess etch and a gate metal thickness of 2250 Å. The gate level was patterned by EBM-VI.

The resistances and current density handling capability of the various metallizations shown in (A) of Table 3 are typical. All are considered to have adequate current carrying capability. (B) shows the yield of 8 serially connected gateless FETs. (C) shows the yield of the gate stripe shared by five closely spaced test FETs. Pads at each end of the gate stripe are used to test for electrical continuity. The gate resistance is in a reasonable agreement with the data shown in (A). The gate stripe yield is typical of that observed on other slices. (D) shows contact resistance results. The specific contact resistance, r_c, is larger than the 10^{-6} Ω-cm^2 typically observed on VPE or Si-implanted slices, but does not appear to significantly affect circuit performance (see Table 6). The activation efficiency as deduced from the contact resistance pattern is not in agreement with that obtained from the C-V profile. The difference is believed to be caused by the existence of interface states at the nitride/GaAs interface, which partially depletes the underlying active layer. The interface state density appears to be independent of processing procedures and/or whether a "free" GaAs surface or a nitride covered surface is used.

Isolation results, shown by (E), are acceptable and typical of B^+ -implant isolation. (F) shows diode string yield and electrical characteristics. (G) shows the barrier height obtained from [illegible] data taken on the CV structure used for profiling the doping concentration. The barrier height is in the normal range. (H) shows the average mobility as determined from fat-FET measurements. The average mobility for this ion implanted slice

Table 3

Slice Data

Lot C-5, Slice 80C1-40(60)

Substrate: Cr doped ⟨100⟩ Bridgman (Ingot No. M-5-45)

Se^+ Sheet Implant: 5.0 at 360 and 1.5 x 10^{12} cm^{-2} at 150 keV

Isolation: B^+ implant

A. Metallization Resistance

	ohm/sq.	J_{max}, mA/ μm
Ohmic metal:	2.70	10
Gate metal:	0.20	30
First-level metal:	0.10	50
Second-level metal:	0.09	20

B. Metallization Mimic: 20 of 20 good

C. Gate Stripe Yield

0.5 x 320 μm:	18 of 31 good	$R \cong 155\ \Omega$, $I_{max} = 50$ mA
1.0 x 320 μm:	27 of 27 good	$R \cong 85\ \Omega$, $I_{max} = 80$ mA

D. Contact Resistance: $R_c = 0.82\ \Omega$-mm, $R_\square = 650\ \Omega/\square$, $L_T = 2.5$ μm

$r_c = 10.3 \times 10^{-6}\ \Omega\text{-cm}^2$

Activation efficiency: ∿ 43% (from contact resistance pattern)
∿ 72% (from CV profile)

E. Isolation Across 6 μm Gap at 10 V: (ohmic contacts) 2 and 10 μA/mm without and with lights

F. Three-diode String: (20 μm wide)
15 of 15 good
$R_{(series)} = 600\ \Omega$
$n \cong 1.3$
$V_{(intercept)} = 2.0$ V
Reverse leakage = 1 μA at 18 V

G. Barrier Height: $\Phi_B = 0.78$ eV, $n = 1.2$

H. Average Mobility: $\mu = 2925\ cm^2\ V^{-1}s^{-1}$

I. Via Test Pattern Yield: (50 serial vias) 10 of 16 good for 5 x 10 μm vias;
J_{max} ∿ 30 mA/μm

J. Interconnect Yield: (50 serial first-level metal to gate-level interconnects) — 2 μm lines - 21 of 23 good; $J_{max} \approx 60$ mA/

K. Overlay Capacitor Yield: 9 of 9 good (area = 0.1 mm^2)

L. Crossover Yield:

		$R_{\square}$, Ω/□
1. Gate over active regions:	10 of 10 good	0.14
2. Second-level metal over first-level metal:	10 of 10 good	0.08
3. Second-level metal over gate metal:	9 of 9 good	0.08
4. Second-level metal over polyimide islands:	16 of 16 good	0.09

M. 100 μm Test FETs (W = 100 μm): 18 x 18 mm field (3 x 3 master fields)

	$I_{D_{max}}$ at V_G = +0.7 V (mA)	I_{DSS} (mA)	V_P (V)	g_m (ms)	R_{ON} Ω
SW corner	33	25	2.2	10	75
NW corner	38	30	2.6	12	65
NE corner	38	30	2.6	12	60
SE corner	38	30	2.5	12	60
Center	35	27	2.5	12	60

N. 100 μm Test FET (W = 100 μm): Same master field near center of slice

Subfield	$I_{D_{max}}$ (mA)	I_{DSS} (mA)	V_P (V)	g_m (ms)	R_{ON} (Ω)
A3	34	25	2.5	12	60
B3	35	27	2.5	12	60
C3	34	26	2.6	11	60
A2	35	27	2.5	12	60
B2	35	26	2.5	12	60
C2	34	26	2.5	12	60
A1	36	28	2.5	11	60
B1	37	29	2.5	11	60
C1	36	29	2.5	10	60

O. Current Proportionality Test: I_{DSS} values at 2.5 V in mA

	Width in μm					r	Slope (mA/μm)
	100	80	40	20	10		
SW corner	25.0	20.0	9.8	5.4	3.0	0.9997	0.245
NW corner	30.0	22.5	12.0	6.5	3.5	0.9983	0.287
NE corner	30.0	24.0	12.0	6.6	3.5	0.9999	0.294
SE corner	30.0	23.0	12.5	6.8	3.8	0.9991	0.285
Center	27.5	21.5	11.6	6.0	3.3	0.9996	0.265

is less than that typically obtained on VPE material (~ 4500 cm^2 μs^{-1} cm^{-1}). The yield for the via test pattern (see I) on this slice was inferior to that typically obtained. Typically, the yield of 4 and 3 by 4 μm vias is 40% and ~ 50%, respectively, on most slices. The current density handling capability of the vias is considered adequate. The interconnect yield, shown by (J), as well as the current density handling capability is deemed adequate. (K) shows the yield of the overlay capacitor. Typical yields for such structures are > 95% suggesting a pinhole density < 50 cm^{-2}.

On another slice, the capacitance was mapped. The mean capacitance was 1.83pf with a standard deviation to mean ratio of 3% which suggests acceptable polyimide thickness variation. The relative dielectric constant for the polyimide was determined to be 3.70, in close agreement with the manufacturer's specification, confirming that it is thoroughly cured. The temperature coefficient of the polyimide was measured to be -0.8%/°C which makes its use for filter capacitor applications unlikely.

The crossover yield pattern (see L) consists of a 2.5 x 1250 μm meander line with 110 crossing. The crossover yields have always been good even when the mesa isolation technique is employed.

The results of measurements on test FETs are shown in (M) through (O). The long-range uniformity results are shown in (M). The associated profiles of these same subfields are shown in Figure 10. The correlation between the profiles and FET characteristics is good. The uniformity of device characteristics is adequate for digital circuit applications, as suggested by the yield data that follow. (N) shows the medium-range uniformity results, which are quite good. (O) shows the local uniformity. Here, the scaling of device current with device width is reasonably linear, as evidenced by the correlation coefficient, r. The slope data agree with the data of (M).

B. Yield

To permit a detailed yield analysis of the circuits on Mask set C, the ring oscillators on both slice 80-C1-40(60) and slice 80-C1-58(29) were not closed, but rather brought out to two closely spaced pads. Slice 80-C1-58(29) was scribed, and chips were mounted in 28-pin packages for evaluation. The

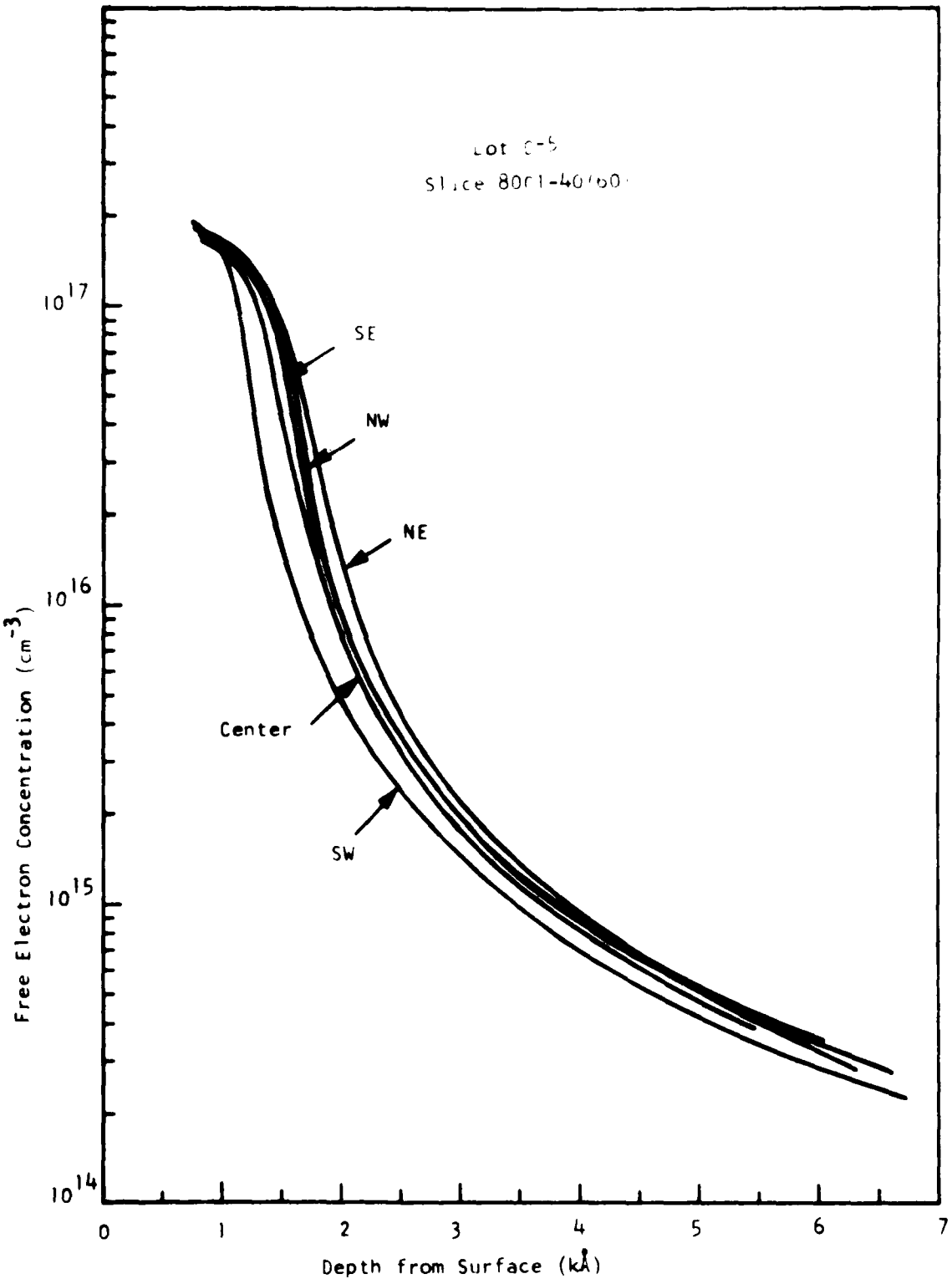


Figure 10 Profiles of Subfields Associated with the Test FETs Shown in Table 3 (M)

overall yield was ~ 75% for the six-stage inverter chains. The criterion used to define a "good" circuit is its transfer characteristic, which should be of the type shown by Figure 11. Note the oscillations at the transition points. They are believed to be the result of capacitive feedback across the two closely spaced pads.

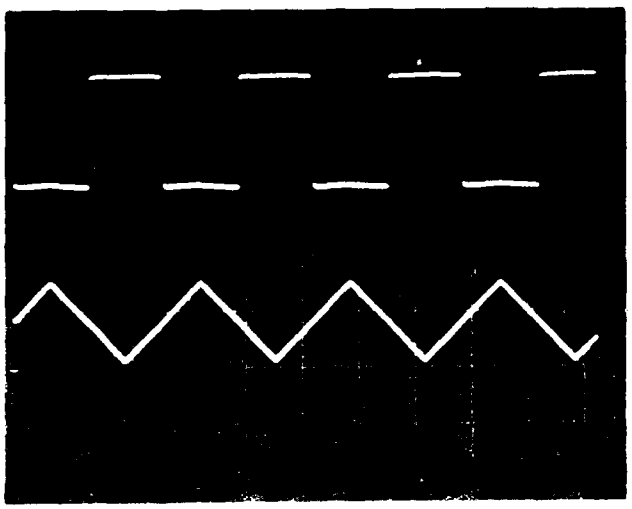
For a more detailed yield assessment, slice 80-C1-40(60) was evaluated in slice form. All 12-stage inverter chains on the slice were probed. The results, summarized in Table 4, clearly indicate the need for improved yield of 0.5 μm circuits. The data also suggest that yield loss due to all factors other than the gate level step is ~ 25%.

C. Power Dissipation

Table 5 shows the power dissipation of the different inverter configurations (see Figure 7). The results were obtained from measurements on functional 12-stage inverter chains and clearly show the dependence of the mean of the power dissipation on pinch-off voltage. Reasonable agreement between the slices is obtained when the power dissipation is normalized either to the square of the pinch-off voltage (including the barrier height) or to the charge underlying the gate. Normalizing the power dissipation to circuit (a), the power dissipation of circuits (b) and (c) are ~ 80% and ~ 55%, respectively. The ratio of standard deviation to the mean of the power dissipation suggests the need to continue to improve long-range material uniformity.

D. Low Temperature Characterization

Results described in this sub-section were obtained from single stage inverters using Mask set B. The active layer concentration of ~ 5.5 x 10^{16} cm^{-3} was obtained by S-doping of the epitaxial layer atop an undoped buffer layer of ~ 3 μm (both grown sequentially by VPE on a Cr-doped, Bridgman substrate). Average mobility of measurements for this slice ranged from 4400 to 5400 cm^2 V^{-1} S^{-1} at 300 K. R_μ ranged from 1.03 to 1.07. This slice, as well as many other slices, exhibit mobility peaks lying between 300 and 77 K. [This temperature is estimated to be about 160 K.] The ratio of the peak mobility to the mobility at 300 K of this slice ranged between



H = 200 μs/div

H = 20 μs/div

Output: Upper Trace
Input: Lower Trace
V = 1 V/div (all)

Figure 11 Transfer Characteristic of Five-Stage Inverter Chain

Table 4

Yield Table for 12-Stage Inverter Chains

Lot: C-5 Slice: 80 C1-40(60)

A. Dependence on gate length, L

L = 0.5 μm	:	39 (57)	%
L = 1.0 μm	:	69 (88)	%
L = 1.5 μm	:	76 (80)	%

B. Positional Yield

Left side of slice	:	74 (80)	%
Center of slice	:	67 (86)	%
Right side of slice	:	44 (57)	%

C. Overall Yield: 60 (76) %

Notes

Number in parentheses excludes marginal circuits

Sample size: 84 (66) circuits

No significant dependence of yield upon circuit type or of yield upon fanout was observed.

Table 5

Power Dissipation of Different Inverter Configurations

(Measured on 12-Stage Inverter Chains)

T = 300 K

	Inverter Configuration	A	B	C
Slice: 80 C1-40(60) Lot: C-5 V_p range: 2.2 to 2.8 V $\langle g_m \rangle$ = 10 mS $n_{peak} = 2.5 \times 10^{17}$ cm^{-3} $\phi_T = 3.43 \times 10^{12}$ cm^{-2}	Sample size	8	24	18
	$\bar{P}_d$, mW (per inverter)	61.7	54.4	35.6
	$\sigma/\bar{P}_d$, %	5	9	20
	$\bar{P}_d/(V_p + \phi_B)^2$, mW-V^{-2}	5.66	5.00	3.27
	$\bar{P}_d/\phi_T$, mW-cm^2	18.0	15.9	10.4
Slice: 80 C1-58(29) Lot: C-6 V_p range: 1.2 to 1.8 V $\langle g_m \rangle$ = 9.7 mS $n_{peak} = 1.2 \times 10^{17}$ cm^{-3} $\phi_T = 1.90 \times 10^{12}$ cm^{-2}	Sample size	3	8	4
	$\bar{P}_d$, mW (per inverter)	36.2	27.5	19.0
	$\sigma/\bar{P}_d$, %	5	19	14
	$\bar{P}_d/(V_p + \phi_B)^2$, mW-V^{-2}	6.84	5.20	3.59
	$\bar{P}_d/\phi_T$, mW-cm^2	19.1	14.5	10.0

1.20 and 1.23. No significant difference (~ 7%) in C-V profiles at 300 and 77 K were observed for the few slices so characterized. This observation is further supported by the van der Pauw measurements at 300 and 77 K (concentrations typically within ± 15%). The long range and medium range uniformity for this anodically thinned slice was acceptable as evidenced by the data presented in Table 1.

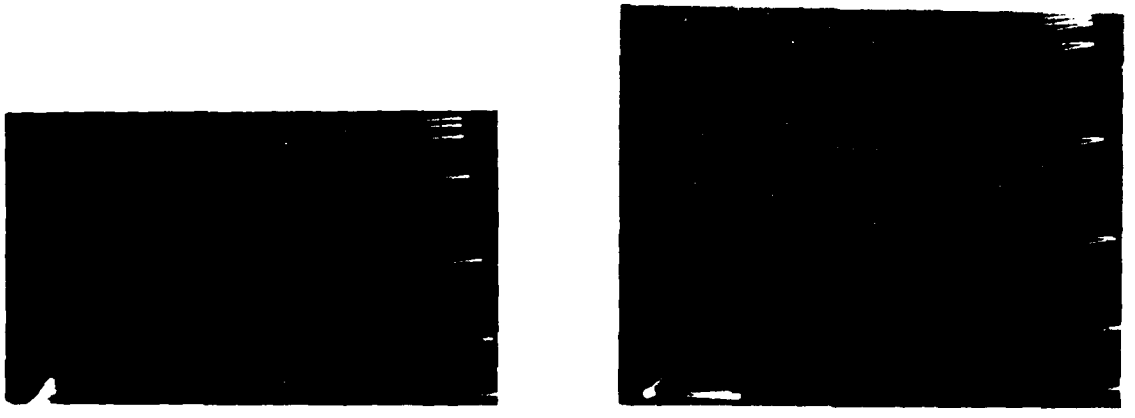
1. Low Frequency Characterization

Chips were mounted in 28-pin packages for low frequency and low temperature characterization. The test FETs, logic branches, and voltage shifter branches were characterized at 300 K and 77 K. Figure 12 is an example of such characterization for the logic branch. The transition points of these circuits conform to expectation (see Figure 7). Other features are noteworthy. First, from test FET characteristics, I_{DSS} increases by 46% at 77 K compared to 300 K. This is reflected by the characteristics shown in Figure 12, where the logic branch current at zero gate voltage increases by ~ 35%. Second, R_{on} decreases by ~ 15%, while the transconductance increases by ~ 20%. Third, the transition point of the logic branch is not significantly altered. Fourth, the sum of the pinch-off voltage and built-in voltage increases by ~ 16% at 77 K compared to that at 300 K.

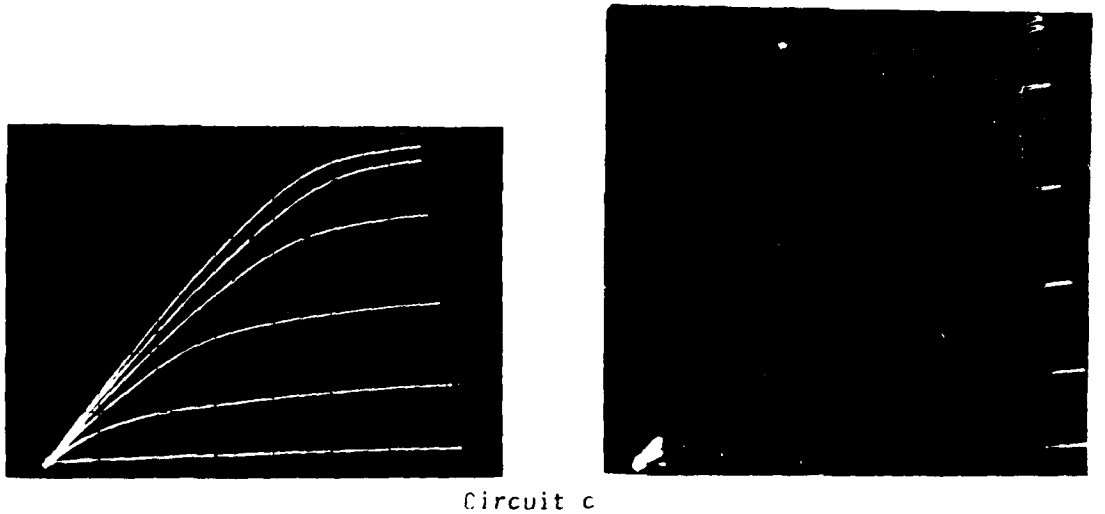
The transfer characteristics and power dissipation of the inverters were assessed next. A typical transfer characteristic is shown in Figure 13(a). An input triangular waveform that ramps between 0.7 and -2.5 V at 1 kHz was used. The circuit bias supplies were adjusted to result in output levels at 0.7 V and -2.5 V. Voltage gain for circuits (a) and (b) was typically between 4 and 5, while that for circuit (c) was usually about 2.5. The transfer characteristics are unchanged over the 1 Hz to 1 MHz frequency range. At 77 K, without changing the bias supplies, the upper output level decreased to ~ 0 V, as shown by Figure 13 (b). The output levels were recovered by readjusting the bias supplies; Figure 13 (c). The increase in power dissipation is typically about 80 to 90%.

300 K

Circuit a



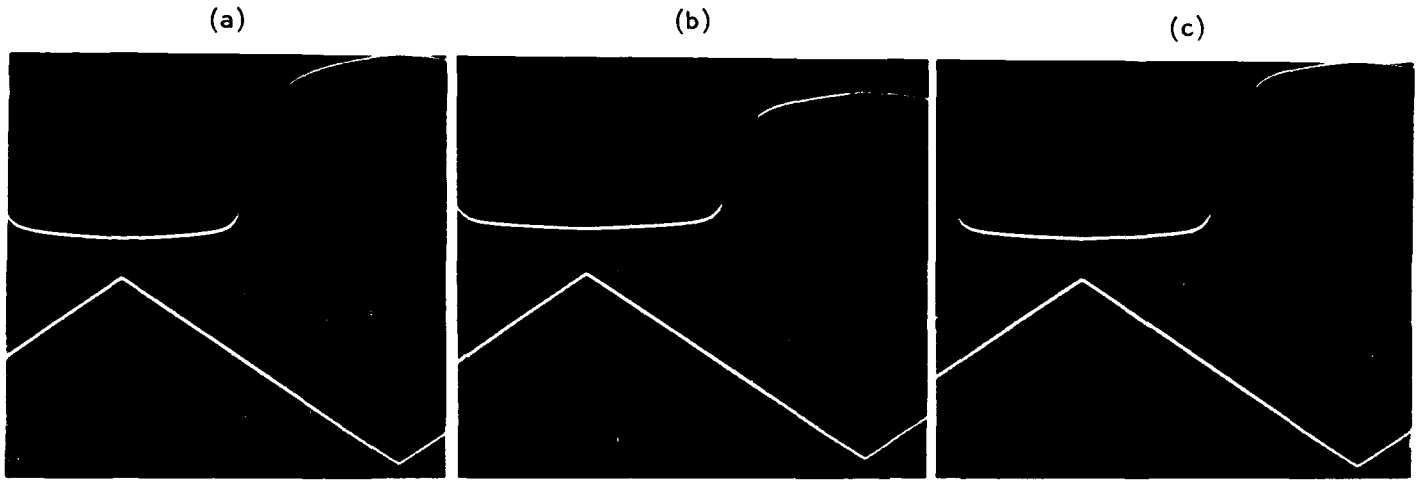
Circuit b



Circuit c

All traces: V = 0.5 mA/div [illegible] div
Step 0.5 V [illegible]

Figure 12 Logic Branch Characteristics at [illegible] for Lot 11, Device 715-2



Voltage-Current Conditions (Square Wave Input) for Dissipation

T (K)	V_{DD} (V)	V_{SS} (V)	I_{DD} (mA)	I_{SS} (mA)	I_{gr} (mA)	P_{diss} (mW)
300	5.757	3.84	4.33	3.10	1.23	36.8
77 (before bias adjustment)	5.752	3.84	7.11	4.49	2.63	58.2
77 (after bias adjustment)	6.516	4.02	7.97	4.66	3.30	70.6

Figure 13 Inverter Transfer Characteristics at 300 and 77 K. Lot 11, device 715-1, circuit b.

2. High Frequency Characterization

Microstrip circuit arrangements shown in Figure 14 were used for testing at high frequencies. A 10 kΩ chip resistor was used to avoid excessive loading of the output, and the bias lines were shunted to ground through a 0.01 μF chip capacitor. The test equipment set-up employed is shown schematically in Figure 15. The circuits were first tested in the low frequency setup to ascertain the appropriate bias conditions before testing in the high frequency setup. The response of an inverter to a 0.55 GHz sine wave of 3.2 V peak-to-peak is shown in Figure 16 (a) through (c) for gate bias of -0.65, -1.25, and -0.25 V, respectively. Here a circuit (b) from lot 11 was employed, and bias conditions were identical to those at low frequency. Note that the response waveform changed in the expected manner with gate bias. Such means, among others, were always employed to verify proper circuit action. Figure 16 (d) shows the response to a 2.4 GHz input signal. Good clipping action with rise and fall times of ~ 100 ps was still obtained. At 4.0 GHz [Figure 16 (e)] clipping action is no longer observed, suggesting that it is the upper frequency limit for this particular circuit. However, at 77 K [Figure 16 (f)], clipping action is again observed, with rise and fall times improved to ~ 50 ps. Figure 16 (g) shows the response to a 4.0 GHz signal by a circuit (b) from the same slice with 0.5 μm gate lengths. Unlike the 1 μm gate length circuit [Figure 16 (e)], clipping action is evident, and rise and fall times are improved by a factor of about two. It is significant that the 0.5 μm circuits have been operated at frequencies up to 8.0 GHz. The response becomes increasingly more "sinewave-like" with a gradually decrease in amplitude as the frequency is increased. It is not known at present if this behavior is due to the bandwidth limitation of the measuring system (14 GHz) or due to the circuit itself. Finally, for circuits having the same gate length and with no fan out, preliminary results indicate that the performance of all the circuit configurations shown by Figure 7 is not significantly different (less than a factor of ~ 1.5).

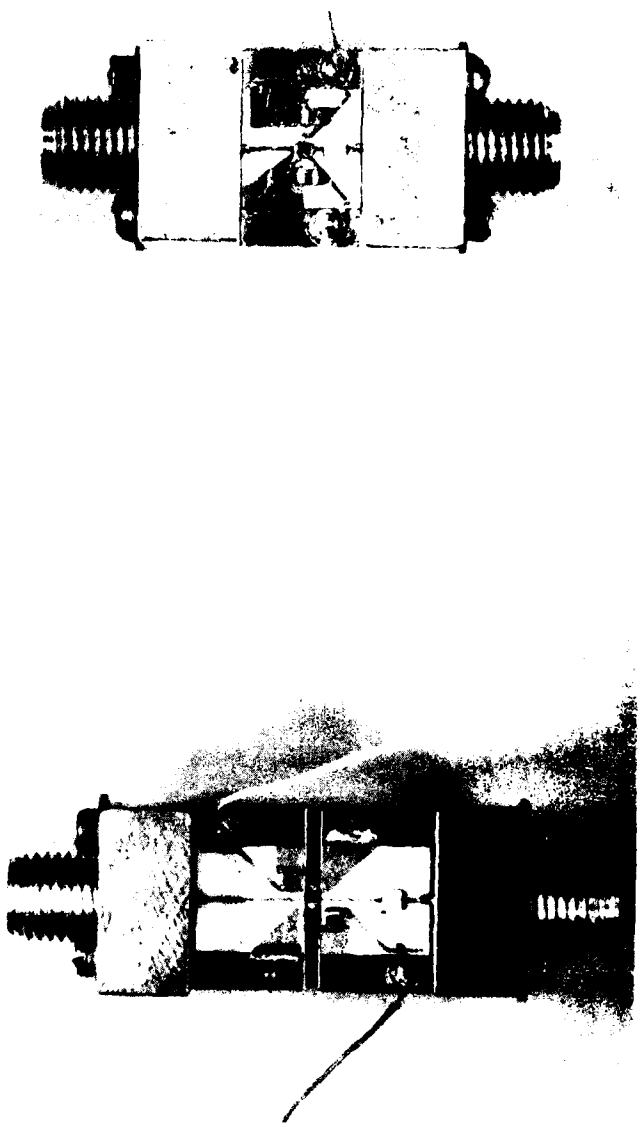


Figure 14 Microstrip Circuit Arrangements for High Frequency Tests. The ceramic microstrip circuits are 7.5 mm square.

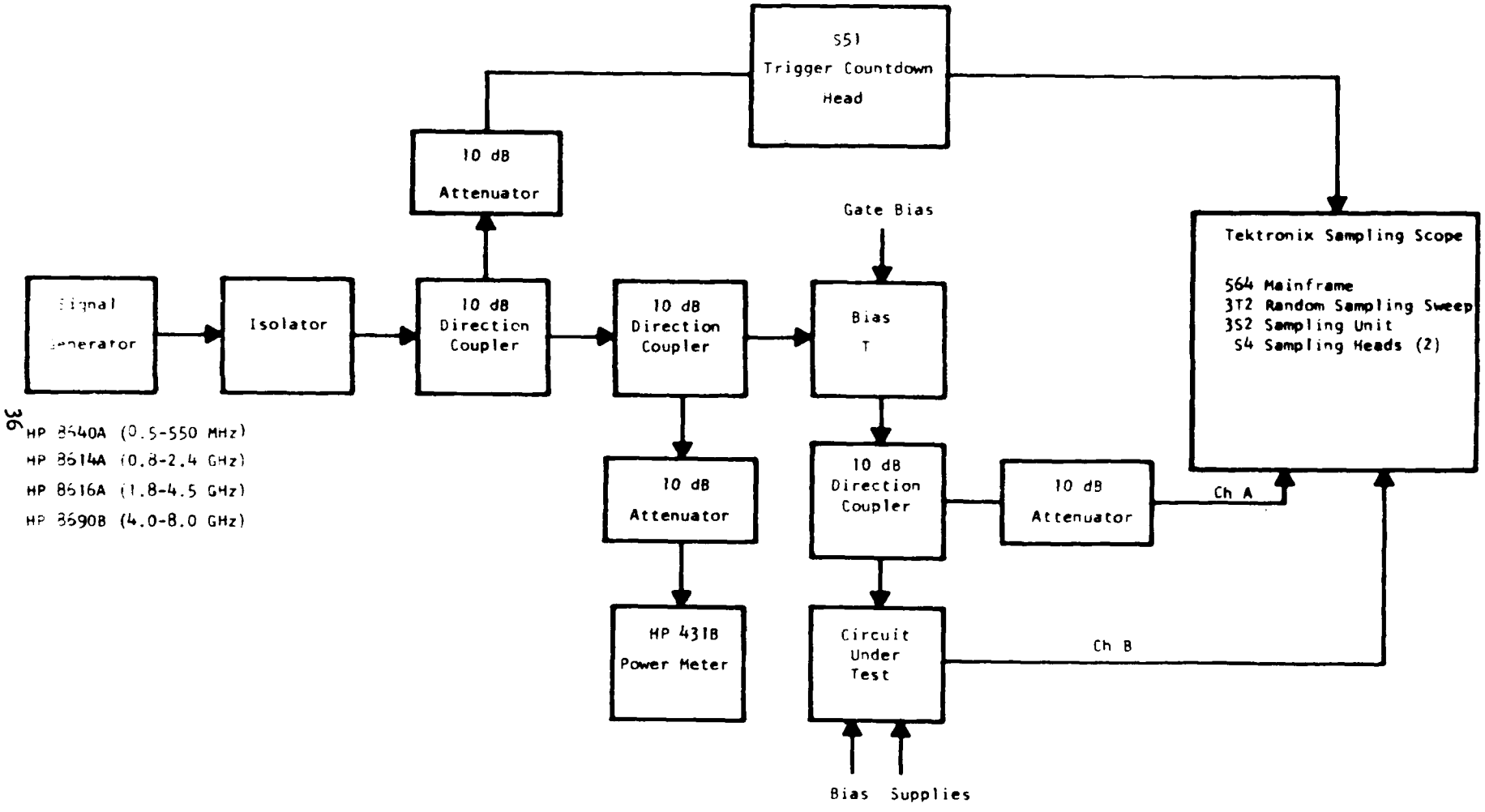
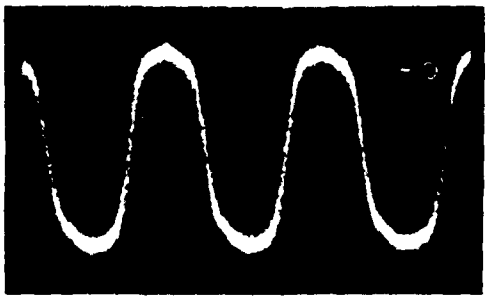


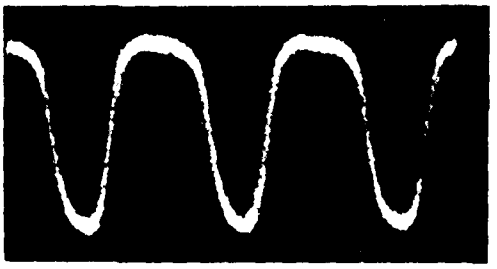
Figure 15 Schematic of Test Equipment Setup

(a) f = 0.55 GHz
V_g = -0.65 V



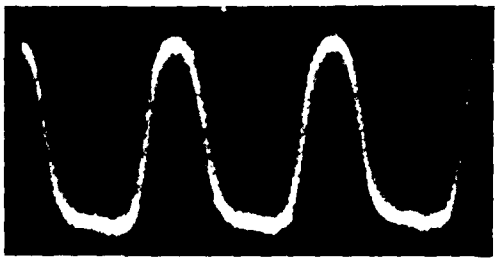
V 1 V H 500 ps

(b) f = 0.55 GHz
V_g = -1.25 V



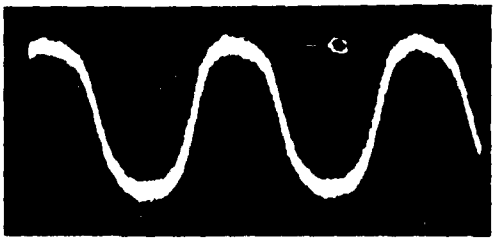
V 1 V H 500 ps

(c) f = 0.55 GHz
V_g = -0.25 V



V 1 V H 500 ps

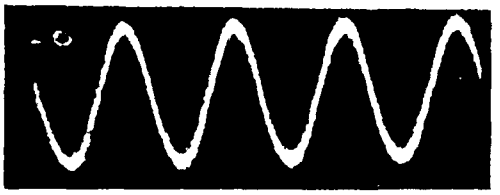
(d) f = 2.4 GHz



V 1 V/div H 100 ps/div

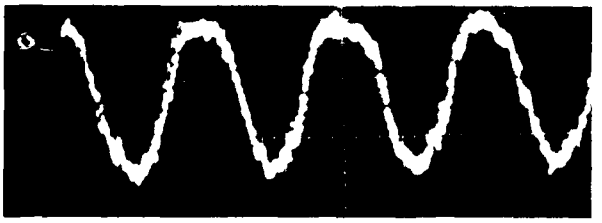
Figure 16 Inverter Response to Sine Wave Inputs. All are for circuit (b) with source-drain spacing of 5 μm. (a) through (f) are for the same circuit with L = 1 μm, while (g) is for an L = 0.5 μm circuit. T = 300 K except for (f). For all cases, no fanout loads were employed.

(e) f = 4.0 GHz



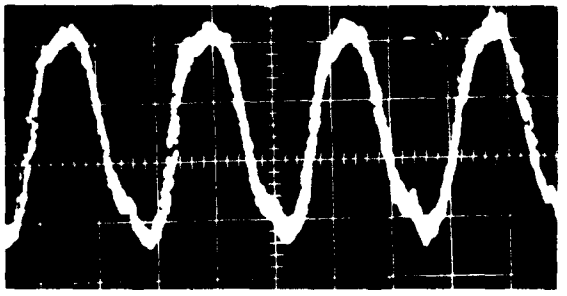
V = 1 V H = 100 ps

(f) f = 4.0 GHz
T = 77 K



V = 1 V/div H = 100 ps

(g) f = 4.0 GHz
L = 0.5 μm



V = 1 V/div H = 100 ps/div

Figure 16 (continued)

By suitable arrangement of the input and output lines (semi-rigid coaxial cables are used), the circuits were operated at 77 K simply by immersion into LN_2. As at low frequencies, the power dissipation at 77 K was 80 to 90% greater than at 300 K. The total arrangement withstands at least two temperature cycles without any alteration in electrical performance.

3. Discussion

The observations that the mobility and concentration profiles are approximately the same at 300 and 77 K while the I_{SAT} value is ~ 46% greater at 77 K compared to that at 300 K suggest the saturation velocity at 77 K is also approximately 46% greater at 77 K than at 300 K. This is supported by comparing the first two lines of the power dissipation data shown in Figure 13 where the power dissipation increased by 58%.

The observation that the sum of the pinch-off voltage and the barrier height, V_p', increases by ~ 16% at 77 K compared to that at 300 K is also reflected by the last two data lines of Figure 13. V_{DD} and V_{SS} were increased by 13% and 5%, respectively, to recover the initial output logic levels; I_{DD} and I_{SS} also increased correspondingly. Since power dissipation varies approximately proportionately to $I_{SAT}\ V'_p{}^2$, the power dissipation would be expected to increase $(1.46)(1.16)^2 = 1.96$ which is in reasonable agreement with the 92% increase actually observed.

The reason for the increase in V_p' is not completely clear. The CV profile at 77 K is shifted to the right (away from the surface) of the 300 K profile by ~ 7%. This could be interpreted to mean either the dielectric constant has decreased by 7% or some electron traps present at 300 K are no longer effective at 77 K. The first assumption implies a 7% increase in V_p' while the second assumption implies a 14% increase in V_p'. This suggests the second assumption is more likely to be the correct one.

Based on gm ≈ I_{Dmax}/V_p', the device results indicate a speed advantage of ~ 26% can be expected at 77 K compared to that at 300 K. Though qualitative, the measured results to date suggest a much greater speed advantage. The accuracy of comparative speeds is expected to improve substantially with the use of ring oscillators for test circuits.

E. Ring Oscillator High Frequency Results

The inverter chains of slice 80C1-40(60) were converted to ring oscillators (ROs) by shorting the two closely spaced pads. The frequency of oscillation of the ROs was detected with the use of a spectrum analyzer. Bias supplies were adjusted to maximize the fundamental and third harmonic components. Three of each type of circuit (a), one of each type of circuit (b), and two of each type of circuit (c) were sampled. All ROs tested were located in the same slice region. Although the data base is limited, (the slice was lost during additional bonding operations because of operator error) and has not been confirmed by direct waveform observation, a number of useful tentative conclusions can be drawn from the data. The measured propagation delays, shown in Table 6, are averaged values; the data for circuit (b) were not sufficient to be included. The values shown by Table 6 are typically the average of two measurements. These values generally were in agreement to within 20%. Propagation delays obtained from 11-stage ROs were typically about 20% greater than those obtained from the corresponding 5-stage ROs. The yield of operating ROs was comparable to the yield obtained under low frequency test conditions. Uniformity of dc operating voltages and resulting currents was good.

The data of Table 6 are plotted, with some curve smoothing in Figure 17. Preliminary conclusions are given below; however, it should be noted that they are applicable only to the particular circuit layout used. (a) For FO < 4, only a ~ 20% improvement in t_D is obtained when L is reduced to 0.5 μm from 1.0 μm. This is true for both circuit configurations. (b) Circuits with L > 1.0 μm suffer significant speed loss. This degradation increases with increasing FO. (c) The advantage of circuit (a) over circuit (c) in terms of speed is ~ 25% for FO < 2. This advantage increases significantly for FO > 2.

Table 6

Propagation Delay (Picoseconds) vs Gate Length (μm) and Fan-Out

Circuit: 5-Stage ROs Slice: 80C1-40(60)

	Circuit Type	L = 0.5	L = 1.0	L = 1.5	L = 2.0
	a	82	98	12[illegible]	142
FO = 1	c	91	107	147	233
	a	94	113	143	190
FO = 2	c	119	156	192	261
	a	105	123	--	234
FO = 4	c	167	200	313	476
	a	114	202	232	334
FO = 8	c	228	278	667	871
Yield (%)		60	80	75	90

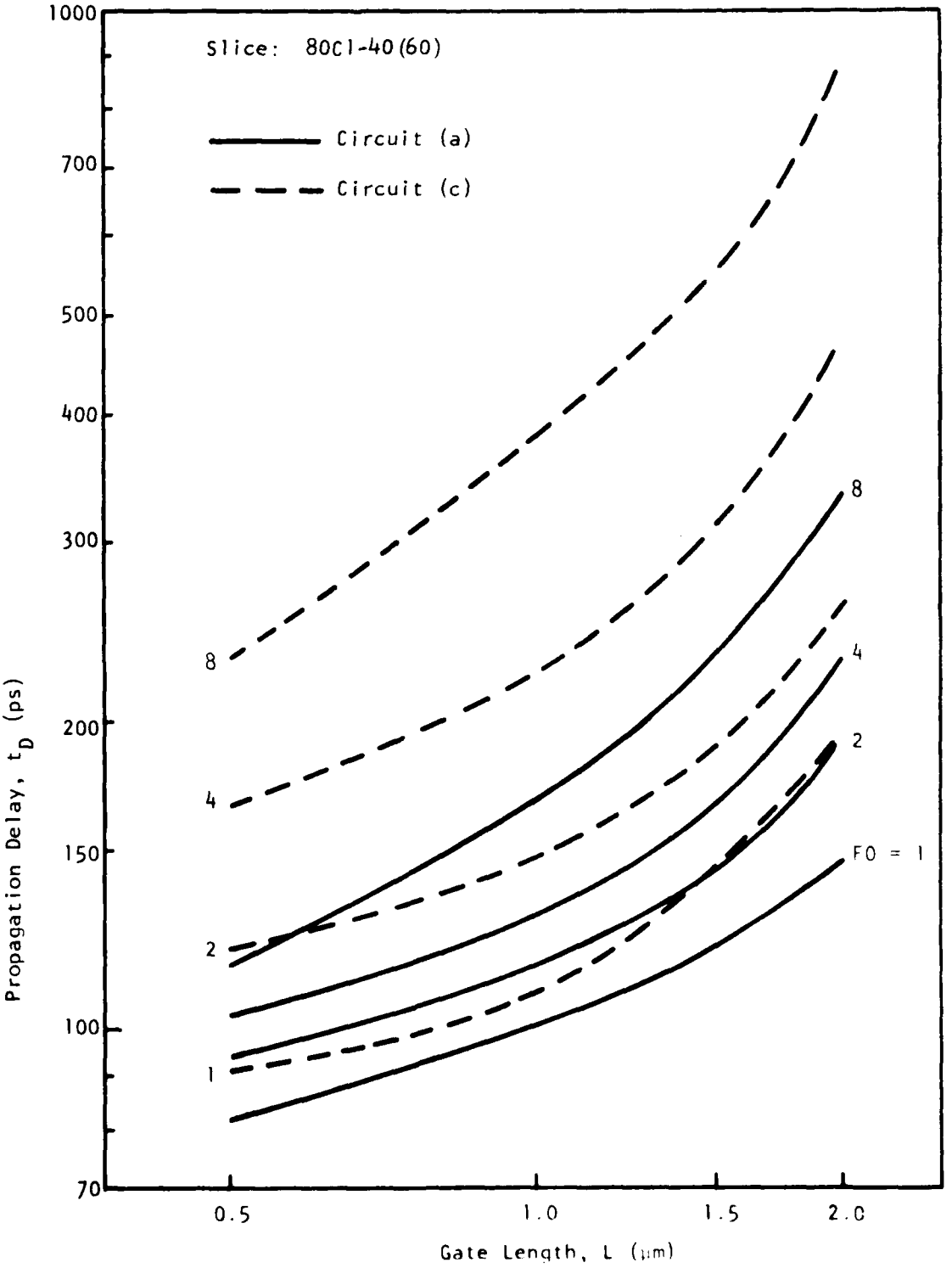


Figure 17 Dependence of Propagation Delay on Gate Length, Fan-Out, and Circuit Type

SECTION VI
MODELING ACTIVITIES

The modeling effort, started at the end of this period, has been directed toward developing a dc model capable of simulating the characteristic curves for a single FET. The best results have been obtained using the model developed by Van Tuyl and Liechti.[2] A program for an HP9845B calculator was written that solves the nonlinear equations using a Newton-Raphson iteration technique. As shown by Figure 18, calculated and measured results are in good agreement.

The inverter logic branch was then simulated by a second program, which models two devices in series. Again, acceptable agreement between calculated and measured results was obtained (see Figure 19). Similar agreement was obtained for circuits (b) and (c).

Plans for the future include modeling a complete inverter stage and studying the effect of device parameter variation on the inverter transfer characteristic and on power dissipation.

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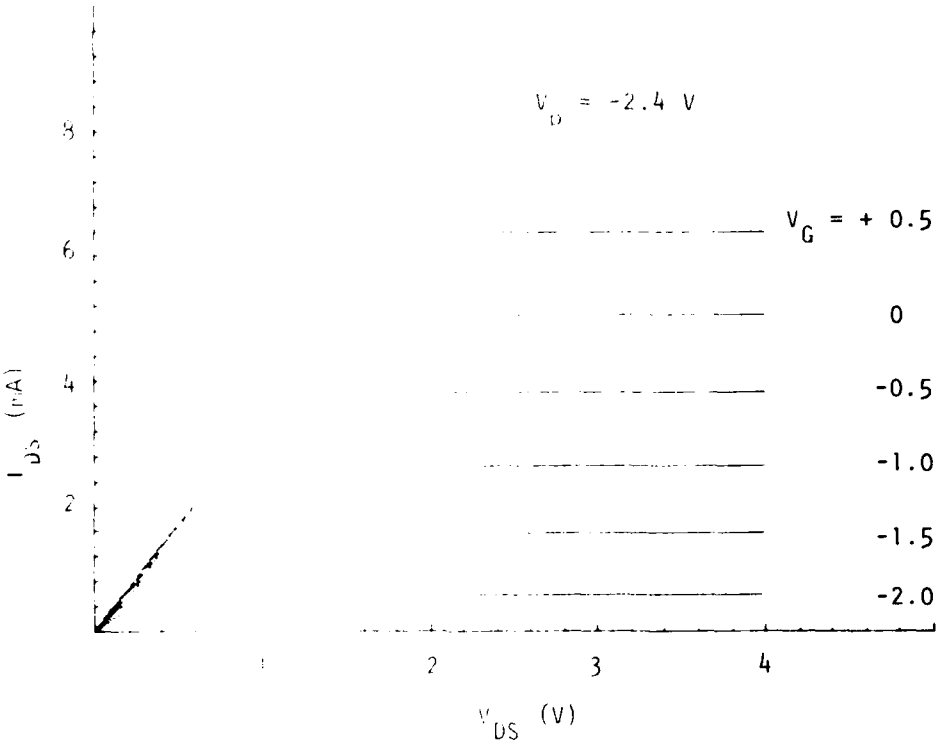
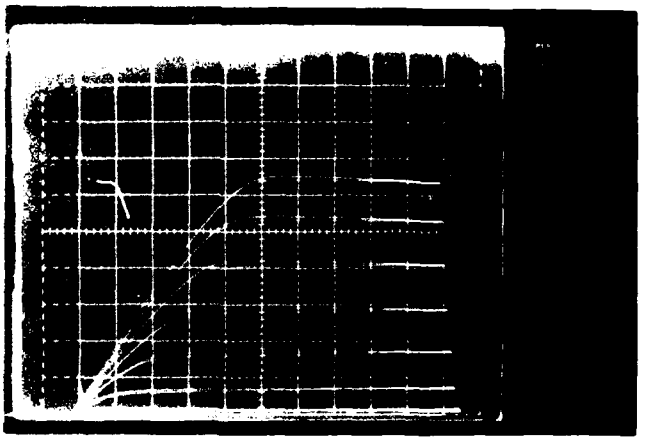
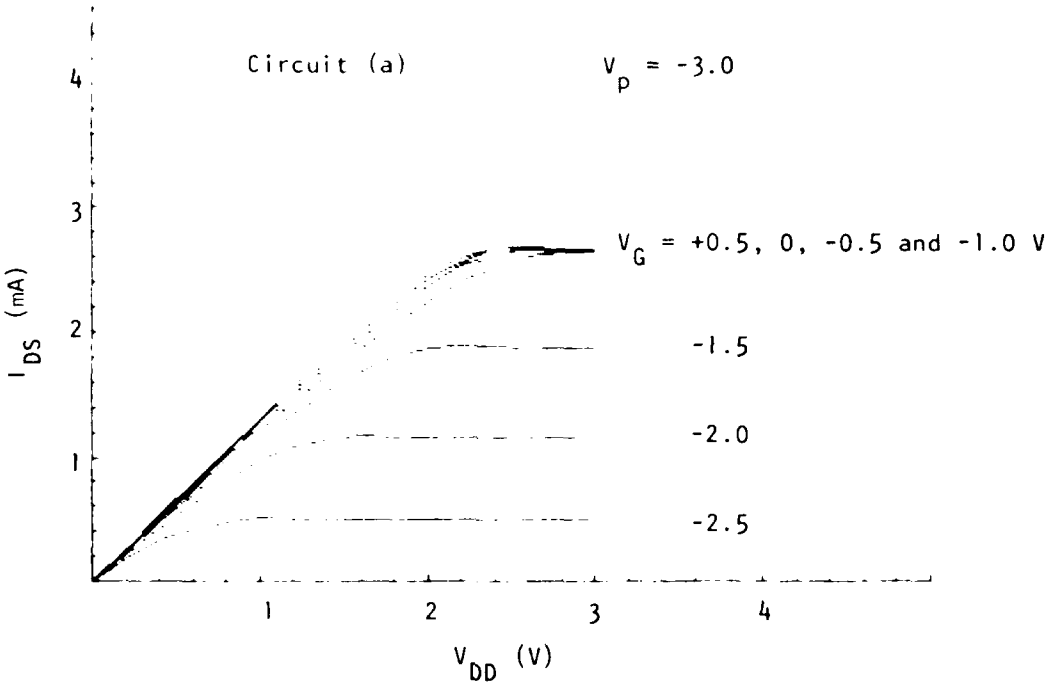
[2]R. Van Tuyl and C. A. Liechti, "Gallium Arsenide Digital Integrated Circuits," Air Force Avionics Laboratory, WPAFB, Technical Report AFAL-TR-74-40, March 1974.

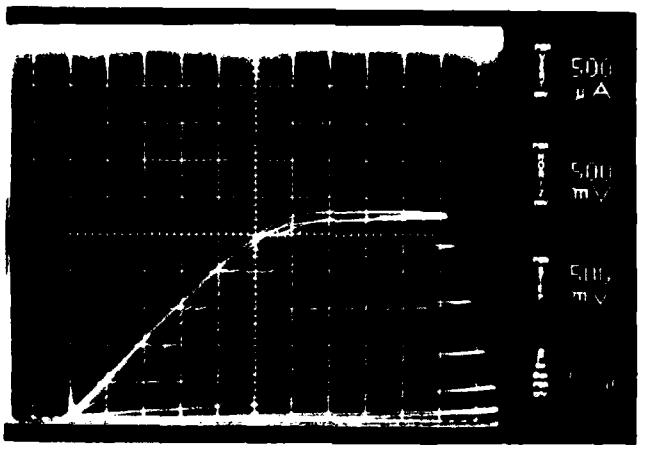




offset = + 0.5 V

Figure 18 Simulated and Measured Results for a 20 μm Wide FET Having a Pinch-Off of -2.4 V. Slice 80C1-40(60).





First Four Traces
Nearly Coincident

Offset = +0.5 V

igure 19 Simulated and Measured Results for Circuit (a) Having a Pinch-Off of -3.0 V. Slice 80C1-40(60).

SECTION VII
SUMMARY

Progress made during the first year of this research program is summarized below.

- High quality VPE layers have been grown that exhibit 300 and 77 K mobilities comparable to those reported in the literature. When anodically thinned, the uniformity of the active layers is adequate for circuit processing.

- A standard, high-yield, reproducible fabrication process has been developed which is suitable for the present research program.

- Procedures for translating circuit concepts into mask sets are adequate to ensure rapid turnaround.

- Material and device/circuit characterization techniques, as well as record maintenance, have been standardized to ensure a continuing expansion of the data base.

- High frequency measurement techniques were well established. On-slice, high frequency measurement techniques at room temperature have been developed. Extension to near 77 K temperatures is planned.

- Modeling activities have been initiated. With further development, these activities are expected to contribute increasingly to the circuit design and layout activity.

The progress made during the past year leads us to believe no serious obstacles to the successful implementation of the research program will be encountered.

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